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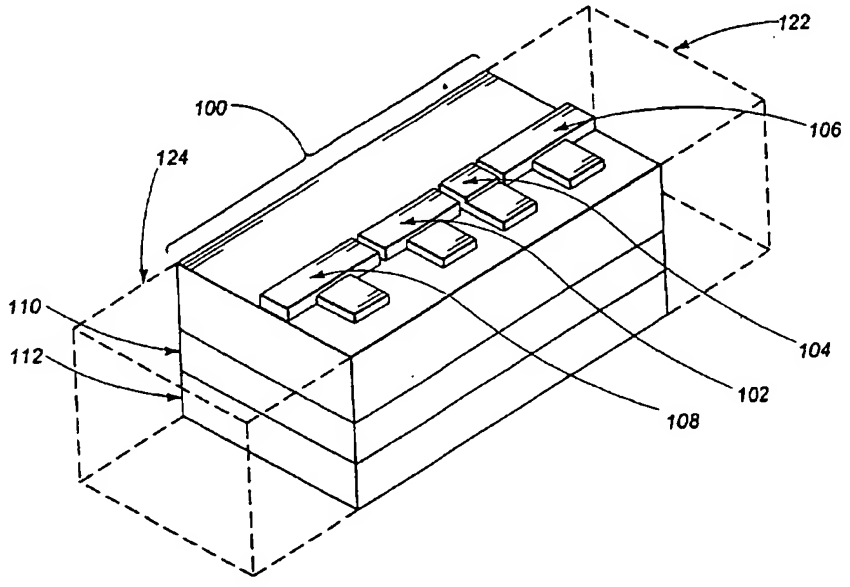
(54) Title: GAIN VOLTAGE CONTROL OF SAMPLED GRATING DISTRIBUTED BRAGG REFLECTOR LASERS




(57) Abstract: A gain voltage controller for use with a sampled grating distributed Bragg reflector (SGDBR) laser is presented. The controller for provides separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser and a voltage monitor, coupled to a gain section of the laser for monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller. The controller controls the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

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# GAIN VOLTAGE CONTROL OF SAMPLED GRATING DISTRIBUTED BRAGG REFLECTOR LASERS

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit under 35 U.S.C. §119(e) of the following co-pending and commonly-assigned U.S. patent applications:

Provisional Application Serial No. 60/215,739, filed June 29, 2000, by Gregory A. Fish and Larry A. Coldren, entitled "OPEN LOOP CONTROL OF SGDBR LASERS," attorneys' docket number 122.4-US-P1;

Provisional Application Serial No. 60/215,170, filed June 29, 2000, by Paul F. Crowder, entitled "POWER AND WAVELENGTH CONTROL OF SGDBR LASERS," attorneys' docket number 122.5-US-P1, and

Provisional Application Serial No. 60/215,742, filed June 29, 2000, by Paul F. Crowder and Larry A. Coldren, entitled "GAIN VOLTAGE CONTROL OF SGDBR LASERS," attorneys' docket number 122.6-US-P1,

all of which applications are incorporated by reference herein.

This application is a continuation-in-part patent application of the following co-pending and commonly-assigned U.S. patent applications:

Utility Application Serial No. 09/848,791, filed May 4, 2001, by Gregory A. Fish and Larry A. Coldren, entitled "IMPROVED MIRROR AND CAVITY DESIGNS FOR SAMPLED GRATING DISTRIBUTED BRAGG REFLECTOR LASERS," attorneys' docket number 122.1-US-U1, which claims the benefit under 35 U.S.C. §119(e) of Provisional Application Serial No. 60/203,052, filed May 4, 2000, by Gregory A. Fish and Larry A. Coldren, entitled "IMPROVED MIRROR AND CAVITY DESIGNS FOR SGDBR LASERS," attorneys' docket number 122.1-US-P1;

Utility Application Serial No. 09/872,438, filed June 1, 2001, by Larry A. Coldren, Gregory A. Fish, and Michael C. Larson, entitled "HIGH-POWER, MANUFACTURABLE SAMPLED GRATING DISTRIBUTED BRAGG REFLECTOR LASERS," attorneys' docket number 122.2-US-U1, which claims the benefit under 35 U.S.C. §119(e) of Provisional Application Serial No. 60/209,068, filed

June 2, 2000, by Larry A. Coldren Gregory A. Fish, and Michael C. Larson, and entitled "HIGH-POWER, MANUFACTURABLE SAMPLED-GRATING DBR LASERS," attorneys' docket number 122.2-US-P1;

Utility Application Serial No. XX/XXX,XXX, filed June 11, 2001, by Gregory A. Fish and Larry A. Coldren, entitled "IMPROVED, MANUFACTURABLE SAMPLED GRATING MIRRORS," attorneys' docket number 122.3-US-U1, which claims the benefit under 35 U.S.C. §119(e) of Provisional Application Serial No. 60/210,612, filed June 9, 2000, by Gregory A. Fish and Larry A. Coldren, entitled "IMPROVED, MANUFACTURABLE SAMPLED GRATING MIRRORS," attorneys' docket number 122.3-US-P1;

Utility Application Serial No. XX/XXX,XXX, filed on same day herewith, by Gregory A. Fish and Larry A. Coldren, entitled "OPEN LOOP CONTROL OF SGDBR LASERS," attorneys' docket number 122.4-US-U1, which claims the benefit under 35 U.S.C. §119(e) of Provisional Application Serial No. 60/215,739, filed June 29, 2000, by Gregory A. Fish and Larry A. Coldren, entitled "OPEN LOOP CONTROL OF SGDBR LASERS," attorneys' docket number 122.4-US-P1; and

Utility Application Serial No. XX/XXX,XXX, filed on same day herewith, by Paul F. Crowder, entitled "POWER AND WAVELENGTH CONTROL OF SGDBR LASERS," attorneys' docket number 122.5-US-U1, which claims the benefit under 35 U.S.C. §119(e) of Provisional Application Serial No. 60/215,170, filed June 29, 2000, by Paul F. Crowder, entitled "POWER AND WAVELENGTH CONTROL OF SGDBR LASERS," attorneys' docket number 122.5-US-P1,

all of which applications are incorporated by reference herein.

## BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to gain voltage control for semiconductor lasers, and particularly, gain voltage control for Sampled Grating Distributed Bragg Reflector (SGDBR) semiconductor lasers.

2. Description of the Related Art.

Diode lasers are being used in such applications as optical communications, sensors and computer systems. In such applications, it is very useful to employ lasers that can be easily adjusted to output frequencies across a wide wavelength range. A diode laser which can be operated at selectably variable frequencies covering a wide wavelength range, i.e. a widely tunable laser, is an invaluable tool. The number of separate channels that can utilize a given wavelength range is exceedingly limited without such a laser. Accordingly, the number of individual communications paths that can exist simultaneously in a system employing such range-limited lasers is similarly very limited. Thus, while diode lasers have provided solutions to many problems in communications, sensors and computer system designs, they have not fulfilled their potential based on the available bandwidth afforded by light-based systems. It is important that the number of channels be increased in order for optical systems to be realized for many future applications.

For a variety of applications, it is necessary to have tunable single-frequency diode lasers which can select any of a wide range of wavelengths. Such applications include sources and local oscillators in coherent lightwave communications systems, sources for other multi-channel lightwave communication systems, and sources for use in frequency modulated sensor systems. Continuous tunability is usually needed over some range of wavelengths. Continuous tuning is important for wavelength locking or stabilization with respect to some other reference, and it is desirable in certain frequency shift keying modulation schemes.

In addition, widely tunable semiconductor lasers, such as the sampled-grating distributed-Bragg-reflector (SGDBR) laser, the grating-coupled sampled-reflector (GCSR) laser, and vertical-cavity lasers with micro-mechanical moveable mirrors (VCSEL-MEMs) generally must compromise their output power in order to achieve a large tuning range. The basic function and structure of SGDBR lasers is detailed in U.S. Patent 4,896,325, issued January 23, 1990, to Larry A. Coldren, and entitled "MULTI-SECTION TUNABLE LASER WITH DIFFERING MULTI-ELEMENT MIRRORS", which patent is incorporated by reference herein. Designs that can provide over 40 nm of tuning range have not been able to provide much more than a couple of milliwatts of

power out at the extrema of their tuning spectrum. However, current and future optical fiber communication systems as well as spectroscopic applications require output powers in excess of 10 mW over the full tuning band. Current International Telecommunication Union (ITU) bands are about 40 nm wide near 1.55 μm, and it is desired to have a single component that can cover at least this optical bandwidth. Systems that are to operate at higher bit rates will require more than 20 mW over the full ITU bands. Such powers are available from distributed feedback (DFB) lasers, but these can only be tuned by a couple of nanometers by adjusting their temperature. Thus, it is very desirable to have a source with both wide tuning range (> 40 nm) and high power (> 20 mW) without a significant increase in fabrication complexity over existing widely tunable designs. Furthermore, in addition to control of the output wavelength, control of the optical power output for a tunable laser is an equally important endeavor as optical power determines the potential range for the laser.

Fundamentally, maximizing the output power, while stabilizing the output wavelength and the maximizing the side mode suppression ratio are very desirable objectives in the control of SGDBR lasers. Thus, there is a need in the art for devices and methods which maximize the power output. The present invention meets these objectives through a novel use of gain voltage control.

## SUMMARY OF THE INVENTION

A gain voltage controller for use with a sampled grating distributed Bragg reflector (SGDBR) laser is presented. The controller for provides separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser and a voltage monitor, coupled to a gain section of the laser for monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller. The controller controls the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

The gain voltage control of the present invention uses feedback from the SGDBR Laser gain section, typically a voltage, to keep the mirrors aligned with the cavity mode of the laser. The feedback is used to align each mirror, and thereby minimizing the

Laser gain section voltage, since the Laser gain section voltage minimum is where the cavity loss is a minimum. By minimizing the gain section voltage, the optical power output for a given operating point is maximized, the output wavelength is stabilized, and the side mode suppression ratio is increased.

Gain voltage control is implemented in a Digital Signal Processor (DSP) by using either a numerical minima search, or a least mean squares (LMS) quadratic estimator, or can be done using analog circuits using a phase locker (PL) circuit.

When gain voltage control is performed using a DSP, the Laser mirror currents are dithered while the laser gain section is monitored. The DSP then uses a numerical algorithm to align the mirrors by locating the minima of the Laser gain section voltage.

To reduce the effects of noise in the sampled gain voltage signal, a LMS estimator is used to effectively filter the noise by using an array of data points to estimate the gain voltage surface. Use of the LMS promotes faster convergence to the gain voltage minima, as well as providing a smoother transition to the gain voltage minima than a straight minima search using only a minima search algorithm.

In addition to the strictly digital approach using only a DSP, which are limited by analog-to-digital conversion rate and digital-to-analog conversion rate, along with the signal-to-noise ratio of the DSP circuitry, analog phase locking circuitry can be used to minimize these limitations. An analog phase locker (PL), which is a high speed, analog-locking loop is used in conjunction with the DSP, to dither the mirror current, measure the gain voltage with a tuned, narrowband amplifier, extract the phase difference between the stimulus and the measured signal, and drive an error amplifier to adjust the mirror current to the gain voltage. The PL error amplifier output is then measured by the DSP, which adjusts the mirror current values to reduce the error to zero. The DSP effectively operates as an integrator function.

Once new currents to the various sections are established by locking to the external wavelength reference for a given channel, the look-up table can be updated so that the system is adapted to small changes in device characteristics as it ages. Also, by using a formula based upon the initial calibration characteristics, the currents for the other desired operating powers and wavelength channels stored in the look-up table can

be updated as well. This insures that desired operating channels can always be accessed over the device's lifetime.

## BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGS. 1A and 1B depict a typical multiple-section, widely-tunable laser as used in the invention;

FIG. 2 is a block diagram of a typical embodiment of the invention;

FIG. 3 illustrates an open loop control system of present invention;

FIGS. 4A - 4B are flowcharts of the incremental and mirror reflectivity peak calibration processes;

FIG. 5 is a block diagram of the current sources used in the controller;

FIG. 6 illustrates a typical current source circuit of the present invention;

FIG. 7 illustrates a typical current mirror circuit of the present invention;

FIGS. 8A - 8C illustrate a typical closed loop power and wavelength control system;

FIG. 9 illustrates the DSP gain voltage control block diagram;

FIG. 10 illustrates the analog gain voltage control block diagram;

FIG. 11 illustrates the analog phase lock circuit block diagram; and

FIG. 12 illustrates the combined operation of analog gain voltage control circuits to correct the outputs to the two mirrors from the open loop digital controller.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following description, reference is made to the accompanying drawings which form a part hereof, and which is shown, by way of illustration, an embodiment of the present invention. It is understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

1. Overview

FIGS. 1A and 1B depict a typical multiple-section, widely-tunable laser 100 as used in the invention. A typical SGDBR laser 100 as used in the invention essentially comprises four sections that allow its unique tuning characteristics. The laser 100 is comprised of a gain section 102, a phase section 104, a back mirror 106 and a front mirror 108. Below these sections is a waveguide 110 for guiding and reflecting the light beam, while the entire device is formed on a substrate 112. In use, bias voltages are connected to the electrodes 114 on the top of the device and a ground is connected to a lower substrate 112. When a bias voltage on the gain section 102 is above a lasing threshold, a laser output is produced from an active region 116.

The front and back mirrors 108, 106 are typically sampled grating mirrors that respectively include different sampling periods 118, 120. The gratings behave as wavelength-selective reflectors such that partial reflections are produced at periodic wavelength spacings of an optical signal carried in the cavity. The front and back sampled grating mirrors 108, 106 together determine the wavelength with the minimum cavity loss through their effective lengths and grating differential; however, the lasing wavelength can only occur at the longitudinal modes of the optical cavity in the waveguide 110. Therefore, it is important to adjust the mirrors 106, 108 and waveguide 110 modes to coincide, thereby achieving the lowest cavity loss possible for the desired wavelength and maximum mode stability. The phase section 104 of the device shown in FIG. 1 is used to adjust the optical length of the cavity in order to position the cavity modes.

Optional back-side monitor 122 and front-side semiconductor optical amplifier (SOA) and/or optical modulator 124 sections are also indicated. Currents are applied to the various electrodes 114 of the aforementioned sections to provide a desired output optical power and wavelength as discussed in U.S. Patent 4,896,325, issued January 23, 1990, to Larry A. Coldren, and entitled "MULTI-SECTION TUNABLE LASER WITH DIFFERING MULTI-ELEMENT MIRRORS", which patent is incorporated by reference herein. As described therein, a current to the gain section 102 creates light and provides gain to overcome losses in the laser cavity; currents to the two differing SGDBR wavelength-selective mirrors 106, 108 are used to tune a net low-loss window

across a wide wavelength range to select a given mode; and a current to the phase section 104 provides for a fine tuning of the mode wavelength. It should also be understood that the sections are somewhat interactive, so that currents to one section will have some effect on the parameters primarily controlled by the others.

Currents and voltages are applied and/or monitored at the optional sections to monitor power or wavelength, or provide amplification or modulation as specified in commonly-assigned and co-pending applications, namely Application Serial No. 09/614,378, filed on July 12, 2000, by Gregory Fish et al., and entitled "OPTOELECTRONIC LASER WITH INTEGRATED MODULATOR,"; Application Serial No. 09/614,377, filed on July 12, 2000, by Larry Coldren, and entitled "INTEGRATED OPTOELECTRONIC WAVELENGTH CONVERTER,"; and Application Serial No. 09/614,375, filed on July 12, 2000, by Beck Mason et al., and entitled "TUNABLE LASER SOURCE WITH INTEGRATED OPTICAL AMPLIFIER," each of which claims priority to Provisional Applications Serial No. 60/152,072, 60/152,049 and 60/152,072, all filed on September 2, 1999; all of which applications are incorporated by reference herein. The current invention operates under the same general principles and techniques as these background inventions.

FIG. 2 is a block diagram of a typical control system 200 embodiment of the invention. In general, the controller 202 applies input signals 204 to the various sections of the laser 206 to operate it and produce a laser output 208 at a desired wavelength. Many factors may influence the laser output 208 and the controller 202 optimally stabilizes the laser output 208 over the life of the laser 206. In closed-loop variants of the control system 200, the controller 202 may monitor the laser 206 and its output via feedback signals 210 and adjust the various laser inputs 204 accordingly. For example, in one embodiment the laser 206 monitors the feedback signals 210 of the multiple-section, widely tunable laser gain section voltage, temperature, and an external reference 212, such as a wavelength locker (e.g. a Fabry-Perot Etalon), via respective feedback signals 210A - 210C. The controller 202 adjusts the laser section currents and temperature to maintain a fixed optical power and wavelength. The Laser temperature is regulated with a cooling device 214, such as a thermo-electric cooler (TEC), via a separate control loop. The laser 206 generates continuous optical output power.

The controller 202 interfaces to the host over a system interface 216, such as a serial or parallel interface. The host commands the operation of the controller 202. The controller 202 regulates the laser optical output power and wavelength and may operate in one of the following control modes:

A. Open loop control using fixed operating points.

B. Power and wavelength control using open loop control's fixed operating points as initial operating points and regulating the optical power and wavelength to a reference thereafter.

C. Gain voltage control using open loop control's fixed operating points as initial operating points and regulating the Laser mirror alignment with the cavity mode thereafter.

D. Regulating power, wavelength, and gain voltage using open loop control's fixed operating points as initial operating points.

Various embodiments of the control modes are detailed hereafter.

2.0 Open Loop Control

FIG. 3 illustrates an open loop control system 300 that sets the laser optical output 208 power and wavelength by setting the laser section current inputs 204 from values in an aging model stored in the controller 202. The current inputs 204 may be applied, for example, to a back mirror (BM), phase (Ph), Gain (Gn), front mirror (FM), and optical amplifier (SOA) sections of the laser 304. The controller 202 regulates the laser temperature to a fixed value by monitoring a sensor 308 and controlling the cooler 214 accordingly. The current input 204 settings or operating points of the various sections of the laser 304 are generated by a calibration routine. The settings are fixed over the lifetime of the product. The choice of the operating current inputs 204, the current sources, and temperature regulator guarantees maximum stability of the optical output wavelength and power over operating lifetime and ambient environmental conditions.

As previously mentioned, the integrated optical amplifier (SOA), like the integrated modulator, is optional and not included on all designs.

2.1 Operating Points

The laser operating points are determined by either an incremental calibration routine or a mirror reflectivity peak calibration routine.

2.1.1 Incremental Calibration

Incremental calibration steps and locks the laser to each channel, such as each ITU wavelength channel using a calibrated wavelength locker as a reference, such as a Fabry-Perot etalon. It steps to the next channel by adjusting the phase current and locking the mirrors to the cavity mode with gain voltage control. Once at the channel, it locks the Laser wavelength to the channel by adjusting the phase current using wavelength control and the laser power to a predetermined set point by adjusting the gain current with power control.

Incremental calibration starts with the mirrors aligned at mirror reflectivity peak 0 and then searches for the next lower channel. At each cavity mode, it resets the phase current to its initial value and continues the search. At the end of each mirror tuning range, the mirror currents are reset to the next mirror reflectivity peak. Once the wavelength wraps around, the process is repeated at mirror reflectivity peak 0 by searching for the next upper channel.

FIG. 4A is a flowchart of the incremental calibration process. The typical process may begin by setting the gain current at a nominal operation current at block 404. The mirrors are set at the next reflectivity peak in a chosen direction (up or down) at block 406. If the wavelength wrapped at block 402, the chosen direction is changed at block 400 and the process begins again. If the wavelength did not wrap, the phase current is set at a minimum operation current at block 410 and the mirrors are locked to the cavity mode at block 412. If the mirrors have reached the end of their tuning range at block 408, the process resets to block 406 at the next reflectivity peak. If the tuning range has not been reached, the power and wavelength are locked at the channel and the mirrors are aligned at block 416. The channel and corresponding input currents are recorded at block 418 and the laser is stepped to the next channel with the mirrors lock to phase at block 420. If the cavity mode has been passed at block 414, the process restarts at block 410 to reset the phase current. If the cavity mode has not been passed,

power and wavelength are locked again at the new channel as the process resets to block 416. This process will continue until a change in wavelength is indicated again at block 400. At this point, the process ends.

The following pseudo-code also describes the logic of the incremental calibration shown in FIG 4A.

```
For each wavelength direction about mirror reflectivity peak 0
Until (wavelength wraps)
    Set gain current at nominal operational current
    Set mirrors at next reflectivity peak
    Until (end of mirror tuning range)
        Set phase current at minimum operational current
        Lock mirrors to cavity mode
        Until (passes cavity mode)
            Lock power and wavelength at channel and align mirrors
            Record channel and currents
            Step to next channel with mirrors locked to phase
```

2.1.2 Mirror Reflectivity Peak Calibration

Mirror reflectivity peak calibration determines the mirror reflectivity peaks, generates the mirror tuning efficiency curves, and uses the curves to set the mirror currents for each channel.

FIG. 4B is a flowchart of the mirror reflectivity peak calibration process. The process may begin with sweeping the mirror with the cavity mode aligned to the mirror at block 424. The gain voltage minima, which correspond to the mirror reflectivity peaks, are located at block 426. The currents corresponding to the minima are recorded at block 428. If the wavelength does not cross the 0 peak at block 422, the process returns to block 424 to continue sweeping the mirror. Otherwise, a mirror tuning efficiency curve is generated from the reflectivity peaks at block 430. Then at block 434 the mirrors are set to a channel using the mirror tuning efficiency curve. The phase section is aligned to the mirrors at block 436 and the wavelength is locked to the channel

using wavelength control at block 438. Finally, the power is locked to the set point using the power control at block 440 and the channel and input currents are recorded at block 442. The process ends when the last channel has been located as checked at block 432.

The following pseudo-code also describes the logic of the mirror reflectivity peak calibration shown in FIG 4B.

```
Until (wavelength crosses mirror reflectivity peak 0)
    Sweep mirror with cavity mode aligned to mirror
    Locate the gain voltage minima, which is the corresponding mirror
    reflectivity peak.
    Record the currents
Generate mirror tuning efficiency curve from reflectivity peaks
Until (step through all channels)
    Set mirrors to channel using mirror tuning efficiency curve
    Align phase section to the mirrors
    Lock wavelength to channel using wavelength control
    Lock power to set point using power control
    Record the channel and currents
```

2.2 Current Sources

FIG. 5 is a block diagram of the current sources 500 used in the controller 202. The Controller current sources 500 drive the phase, mirror, amplifier, and gain sections of the laser 100. The current sources are comprised of a voltage reference 504, individual 16-bit digital to analog converters 506 (DACs), and voltage to current (VI) amplifiers 508. The DACs 506 connect to the digital signal processor (DSP) synchronous serial port 510 (SSP) through a programmable logic device 512 (PLD). The PLD 512 provides a logic interface between the DSP SSP 510 and the DACs 506. The VI amplifiers 508 translate the DAC voltage outputs 514 to proportional current inputs 204 that drive the laser sections.

2.2.1 Voltage to Current Converter

FIG. 6 illustrates a typical current source circuit 600 of the present invention. The voltage to current amplifier is a modified Howland circuit source (MHCS). A current mirror 602 is added to the output stage of the amplifier 604 to increase the drive current beyond that of the amplifier 604 alone. A filter stage 606 is added at the load 608 to reduce noise.

FIG. 7 illustrates a typical current mirror circuit 602 of the present invention. The current mirror inverts the output of the amplifier 604, which requires the source, Vin, at the inverting node of the amplifier 604 of the current source circuit 600.

The current mirror operates at a fixed gain that is determined, primarily, by the ratio of the resistors 702 in the emitter leads of the transistors. An RC compensation network 704 is added to insure stability of the amplifier and current mirror. The gain of the current is variable up to a maximum ratio. The maximum ratio is determined by the additional drift introduced by heating of the transistor 706 and sense resistor 708 and the maximum thermal loss that can be sustained by the transistor 706 and sense resistor 708. If additional gain is required, an additional Qmo and Rmo section can be added to the mirror 602.

3 Power and Wavelength Control

FIGS. 8A - 8C illustrate a typical closed loop power and wavelength control system. FIG. 8A illustrates the control block diagram. Power and wavelength control 800 combines open loop control (as shown in FIG. 3) and feedback 210A from an external wavelength locker (e.g., a Fabry-Perot Etalon) reference 212 to lock the laser optical output power and wavelength to the reference 212. Power and wavelength control compensates for drift in the controller current sources 508 and the laser operating points over time and temperature.

Once new currents to the various sections 304 are established by locking to the external wavelength reference 212 for a given channel, the aging model or lookup table can be updated so that the system is adapted to small changes in device characteristics as it ages. Also, by using a formula based upon the initial calibration characteristics, the

currents for the other desired operating powers and wavelength channels stored in the aging model can be adjusted as well. For example, the currents for each section at any other channel are adjusted in proportion to the change in that section current at the operating channel.

dIgain = Igain,change / Igain,calibration [at operating channel]

change = (Igain,calibration + dIgain * Igain,calibration [at any other channel]

This is done for each section current. This insures that desired operating channels can always be accessed over the device's lifetime.

The power and wavelength controls may each operate independently or interdependently with other laser inputs.

3.1 Independent

FIG. 8B is a flow diagram of independent control of the power and wavelength. The least complex control algorithm is where the controls operate independently. Each control algorithm induces changes in one laser input, such as a current or temperature, independent of the other laser inputs. The control algorithms are classical proportional, integral control routines. The laser output is compared to the reference to identify whether a change in optical power and/or optical wavelength is indicated at block 810. If a change in the optical power is indicated at block 812, the optical power is adjusted by the gain current (Ign) or by the current to a SOA (if integrated into the Laser) at block 814. If a change in the optical wavelength is indicated at block 814, optical wavelength is adjusted by the phase current (Iph) or the submount temperature at block 818. Of course, the order of the power or wavelength adjustment is unimportant. In addition, the aging model may be updated whenever a change (in power or wavelength) is indicated. Mirror currents are left fixed.

3.2 Interdependent

FIG. 8C is a flow diagram of interdependent control of the power and wavelength. The independent control algorithm is slow and marginally stable in its

response to changes in the optical power output and optical wavelength. The mirrors and cavity mode become misaligned as the control algorithm adjusts the gain and phase currents from their predefined values. The quality of the optical output is reduced (decreased side mode suppression ratio) and the probability of a mode hop is increased (wavelength shift) as the mirrors and cavity mode become misaligned.

The interdependent control algorithm induces primary changes in one laser input, such as a current or temperature, and corrects for secondary changes in at least one other laser input with an adaptive filter or estimator. This compensates for wavelength shifts or power changes and mirror misalignment induced when the control adjusts its primary variable. Here also, the laser output is compared to the reference to identify whether a change in optical power and/or optical wavelength is indicated at block 820. If a change in the optical power is indicated at block 822, the power is adjusted by the gain current (Ign) at block 824 and the wavelength is stabilized by adjusting the phase current (Iph) by an adaptive filter at block 826. The mirror currents are realigned by a fixed estimator at block 828. Following this, the aging model is updated at block 836. If a change in the optical wavelength is indicated at block 830, wavelength is adjusted by the phase current (Iph) or the carrier temperature at block 832. The power is stabilized by adjusting the gain current (Ign) by an adaptive filter at block 834. and the mirror currents are realigned by a fixed estimator at block 828. Here too, the aging model is updated at block 836.

The interdependent controls provide more robust, stable, and faster convergence of the power and wavelength to its reference value.

As outlined above, the aging model is then updated to reflect the new model coefficients whereby the currents from the aging model or look-up table are adjusted for a given desired wavelength and power. Also, the changes required for this particular channel can be used to estimate the changes required for all other channels.

4.0 Gain Voltage Control

Gain Voltage Control uses feedback from the Laser gain section voltage to keep the mirrors aligned with the cavity mode. It aligns the mirrors by minimizing the Laser gain section voltage. The Laser gain section voltage minimum is where the cavity loss is

a minimum. It corresponds to maximum optical power output, wavelength stability, and side mode suppression ratio.

Gain voltage control is implemented in the DSP using a numerical minima search or a least mean squares (LMS) quadratic estimator or in analog circuitry using a phase locker (PL) circuit.

4.1 DSP Gain Voltage Control

FIG. 9 illustrates the DSP gain voltage control block diagram. The DSP dithers the Laser mirror currents 902, 904 and monitors the Laser gain section voltage 906. It uses a numerical algorithm to align the mirrors by locating the minima of the Laser gain section voltage.

4.1.1 DSP Minima Search Algorithm

The minima search algorithm uses three data points (mirror current, gain voltage) and estimates the slope of the gain voltage curve with respect to the mirror current. The algorithm steps towards the gain voltage minima and calculates the next data point and uses the new data point and the two best points to re-estimate the slope of the gain voltage curve. The algorithm continues the above step process, continually searching for the gain voltage minima.

4.1.2 DSP LMS Estimator

The minima search algorithm is susceptible to wandering around the gain voltage minima due to noise in the sampled gain voltage signal. The wandering is reflected as drift and noise on the optical signal. The LMS estimator reduces the wander and noise by using an array of data points to estimate the gain voltage surface, in effect, filtering the noise. The LMS estimator converges to the gain voltage minima faster and smoother than the minima search.

For fixed phase and gain section currents, the gain section voltage can be modeled using a causal Volterra series expansion over 2 input signals, the front mirror and back mirror currents. For dithering signals in the sub-100kHz regime, the analog

circuitry and the device itself allow a memoryless model, so a 5-tap adaptive quadratic filter model will suffice.

The LMS estimator can then be achieved using either of two classic adaptive filter update algorithms, a standard gradient descent adaptation (LMS or block LMS algorithm) or a (faster) recursive least squares adaptation (RLS algorithm – based on Newton's Method).

The second approach is used to achieve faster convergence of adaptive linear filters when the signals driving the system do not have sufficient spectral flatness to allow a rapid gradient descent. However, in the case of adaptive linear filters, the gradient descent approach converges just as fast as the RLS approach when white noise can be used to drive the system. Recently published results indicate that comparable rates of convergence can be achieved with adaptive quadratic filters if a minor filter structure modification is used and (pseudo) Gaussian white noise can be used to drive the system.

There are two advantages of this LMS estimator approach. First, an initial tap-vector can be stored along with the 4 drive currents in the laser calibration table in flash memory (resulting in much faster convergence). Second, the adaptation step size can be reduced as the system converges, reducing steady-state misadjustment in the mirror section currents.

4.2 Analog Gain Voltage Control

FIG. 10 illustrates the analog gain voltage control block diagram. The gain voltage 1002 is connected to analog phase lockers (PL) 1004A, 1004B for each mirror section 1006A, 1006B. The digital algorithms are limited in speed and accuracy by the analog to digital converters (ADC or A/D) 1008A, 1008B and digital to analog converters (DAC or D/A) 1010A, 1010B as well as the signal to noise ratio (SNR) of the circuit. The analog phase locker's speed and accuracy is limited by the SNR of the circuit.

FIG. 11 illustrates the analog phase lock circuit block diagram 1100. The analog phase locker is a high speed, analog-locking loop. It is realized by a phase lock loop (PLL) or RF dither locker. The PL works with the open loop control circuit. The output of the PL adds to the output of the open loop control current sources.

The PL uses a high frequency narrowband stimulus 1102 to dither the mirror current. The gain voltage (Vg) 1104 is measured with a tuned, narrowband amplifier 1106. The phase difference between stimulus and measured signal is extracted by a phase comparator 1108 and drives an error amplifier that adjusts the mirror 1110 current to the gain voltage minima and is sampled by an ADC 1112.

The PL error amplifier output is measured by the DSP. The DSP adjusts the mirror current values in the Open Loop Control aging model to reduce the error to zero. The DSP effectively operates as an integrator function.

FIG. 12 illustrates the combined operation of analog gain voltage control circuits to correct the outputs to the two mirrors from the open loop digital controller. The digital memory/DSP 1200 can set a first approximation current and voltage from a table look up. The analog correction circuits 1004A, 1004B can provide feedback and correction signals to the device as described previously, and the digital controller then monitors the correction signals 1202, 1204 and readjusts the currents and voltages to have the feedback currents from the analog correction portions approach zero. The adjusted currents are used by the aging model to update the aging coefficients. This allows for correction of the laser controller over the life of the SGDBR laser, and accounts for changes in operating temperatures and conditions as well as changes in the operation of the SGDBR laser internal components.

## 5 Power, Wavelength, and Gain Voltage Control

Power, wavelength, and gain voltage control operates the power and wavelength control and gain voltage control simultaneously.

## 6 Conclusion

The foregoing description of the preferred embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is not intended that the scope of the invention be limited by this detailed description.

This concludes the description of the preferred embodiment of the present invention. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS:

1. A gain voltage controller for use with a sampled grating distributed Bragg reflector (SGDBR) laser, comprising:

a controller for providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

a voltage monitor, coupled to a gain section of the laser for monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

wherein the controller controls the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

2. The gain voltage controller of claim 1, wherein the controller keeps the front mirror controlled by the front mirror current and the back mirror controlled by the back mirror current aligned with a cavity mode of the laser.

3. The gain voltage controller of claim 1, wherein the controller comprises a digital signal processor (DSP) to control the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

4. The gain voltage controller of claim 3, wherein the DSP dithers the front and back mirror currents.

5. The gain voltage controller of claim 3, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

6. The gain voltage controller of claim 5, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

7. The gain voltage controller of claim 6, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

8. The gain voltage controller of claim 7, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

9. The gain voltage controller of claim 3, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

10. The gain voltage controller of claim 9, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

11. The gain voltage controller of claim 9, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

12. The gain voltage controller of claim 9, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

13. The gain voltage controller of claim 9, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

14. The gain voltage controller of claim 13, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

15. The gain voltage controller of claim 13, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

16. The gain voltage controller of claim 13, wherein the gradient descent adaptation algorithm is an LMS algorithm.

17. The gain voltage controller of claim 13, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

18. The gain voltage controller of claim 9, wherein the LMS estimator is achieved using an adaptive linear filter.

19. The gain voltage controller of claim 9, wherein the LMS estimator is driven by white noise.

20. The gain voltage controller of claim 9, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

21. The gain voltage controller of claim 9, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

22. The gain voltage controller of claim 1, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

23. The gain voltage controller of claim 22, wherein the analog circuit comprises at least one phase locker circuit.

24. The gain voltage controller of claim 23, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

25. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses a phase lock loop.

26. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses an RF dither locker.

27. The gain voltage controller of claim 23, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

28. The gain voltage controller of claim 23, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

29. The gain voltage controller of claim 28, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

30. The gain voltage controller of claim 28, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

31. The gain voltage controller of claim 28, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

32. The gain voltage controller of claim 28, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

33. The gain voltage controller of claim 28, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

34. The gain voltage controller of claim 28, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

35. The gain voltage controller of claim 1, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.

36. A method of controlling a sampled grating distributed Bragg reflector (SGDBR) laser, comprising the steps of:

providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

controlling the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

37. The method of claim 36, wherein the front mirror is controlled by the front mirror current and the back mirror is controlled by the back mirror current aligned with a cavity mode of the laser.

38. The method of claim 36, wherein a digital signal processor (DSP) controls the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

39. The method of claim 38, wherein the DSP dithers the front and back mirror currents.

40. The method of claim 38, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

41. The method of claim 40, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

42. The method of claim 41, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

43. The method of claim 42, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

44. The method of claim 38, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

45. The method of claim 44, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

46. The method of claim 44, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

47. The method of claim 44, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

48. The method of claim 44, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

49. The method of claim 48, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

50. The method of claim 48, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

51. The method of claim 48, wherein the gradient descent adaptation algorithm is an LMS algorithm.

52. The method of claim 48, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

53. The method of claim 44, wherein the LMS estimator is achieved using an adaptive linear filter.

54. The method of claim 44, wherein the LMS estimator is driven by white noise.

55. The method of claim 44, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

56. The method of claim 44, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

57. The method of claim 36, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

58. The method of claim 57, wherein the analog circuit comprises at least one phase locker circuit.

59. The method of claim 58, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

60. The method of claim 58, wherein the at least one phase locker circuit uses a phase lock loop.

61. The method of claim 58, wherein the at least one phase locker circuit uses an RF dither locker.

62. The method of claim 58, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

63. The method of claim 58, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

64. The method of claim 63, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

65. The method of claim 63, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

66. The method of claim 63, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

67. The method of claim 63, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

68. The method of claim 63, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

69. The method of claim 63, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

70. The method of claim 36, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.

71. An article of manufacture embodying logic to implement a method of controlling a sampled grating distributed Bragg reflector (SGDBR) laser, comprising the steps of:

providing separate inputs to the laser including a front mirror current controlling a front mirror and a back mirror current controlling a back mirror to control the laser; and

monitoring a gain voltage of the gain section and providing input of the gain voltage to the controller;

controlling the front mirror current and the back mirror current to minimize the voltage monitored from the gain section of the laser.

72. The article of claim 71, wherein the front mirror is controlled by the front mirror current and the back mirror is controlled by the back mirror current aligned with a cavity mode of the laser.

73. The article of claim 71, wherein a digital signal processor (DSP) controls the front and back mirror currents to minimize the voltage monitored from the gain section of the laser.

74. The article of claim 73, wherein the DSP dithers the front and back mirror currents.

75. The article of claim 73, wherein the DSP uses a numerical minima search to control the front mirror current and the back mirror current and minimize the voltage monitored from the gain section of the laser.

76. The article of claim 75, wherein the numerical minima search comprises using at least three data points of at least one of the front and back mirror currents versus the gain voltage to estimate a slope of a gain voltage curve with respect to the at least one of the front and back mirror currents.

77. The article of claim 76, wherein numerical minima search further comprises a process of stepping toward the gain voltage minima and determining a next data point, identifying a best two points of the at least three data points, and using the next data point and the best two points to re-estimate the slope of the gain voltage curve.

78. The article of claim 77, wherein the numerical minima search further comprises continuously repeating the process such that the next data point and the best two points of a prior process become the at least three data points of a subsequent process.

79. The article of claim 73, wherein the DSP uses a least mean squares (LMS) estimator to control the front mirror current and the back mirror current and determine at least one gain voltage minimum.

80. The article of claim 79, wherein the LMS estimator uses an array of data points to estimate a gain voltage surface.

81. The article of claim 79, wherein the LMS estimator models the gain voltage using a causal Volterra series expansion over the front and back mirror currents for a fixed phase section current and fixed gain section current of the laser.

82. The article of claim 79, wherein the LMS estimator uses a memoryless 5-tap adaptive quadratic filter model.

83. The article of claim 79, wherein the LMS estimator is achieved using an adaptive filter update algorithm.

84. The article of claim 83, wherein the adaptive filter update algorithm is a gradient descent adaptation algorithm.

85. The article of claim 83, wherein the gradient descent adaptation algorithm is a block LMS algorithm.

86. The article of claim 83, wherein the gradient descent adaptation algorithm is an LMS algorithm.

87. The article of claim 83, wherein the adaptive filter update algorithm is a recursive least squares adaptation algorithm.

88. The article of claim 83, wherein the LMS estimator is achieved using an adaptive linear filter.

89. The article of claim 83, wherein the LMS estimator is driven by white noise.

90. The article of claim 83, wherein an initial tap-vector and inputs to the laser are stored in a laser calibration table.

91. The article of claim 83, wherein a step size of the LMS estimator is reduced as the LMS estimator determines the at least one gain voltage minimum.

92. The article of claim 71, wherein the voltage monitor comprises an analog circuit, to control the front mirror current and the back mirror current.

93. The article of claim 92, wherein the analog circuit comprises at least one phase locker circuit.

94. The article of claim 93, wherein phase locker circuits are each coupled to the front mirror and the back mirror.

95. The article of claim 93, wherein the at least one phase locker circuit uses a phase lock loop.

96. The article of claim 93, wherein the at least one phase locker circuit uses an RF dither locker.

97. The article of claim 93, wherein the at least one phase locker circuit is used in an open loop control system for the laser.

98. The article of claim 93, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current and compares the narrowband stimulus to the gain voltage to determine an error input for the controller and the controller uses the error input to control the laser to operate at a minimum gain voltage.

99. The article of claim 98, wherein the at least one phase locker circuit measures the gain voltage with a narrowband amplifier.

100. The article of claim 98, wherein the at least one phase locker circuit uses a phase comparator to determine the error input from the at least one dithered mirror current and the gain voltage.

101. The article of claim 98, wherein the at least one phase locker circuit dithers the at least one mirror current by driving an error amplifier that modifies the at least one mirror current.

102. The article of claim 98, wherein the error input is coupled to an analog to digital converter (ADC) of the controller and the controller uses the digitally converted error input to adjust values in an aging model corresponding to the separate inputs to the laser.

103. The article of claim 98, wherein the at least one phase locker circuit uses a high frequency narrowband stimulus to dither at least one mirror current.

104. The article of claim 98, wherein phase locker circuit outputs are separately added to the front mirror current and the back mirror current.

105. The article of claim 71, wherein the gain voltage controller is operated simultaneously with power and wavelength control of the laser.

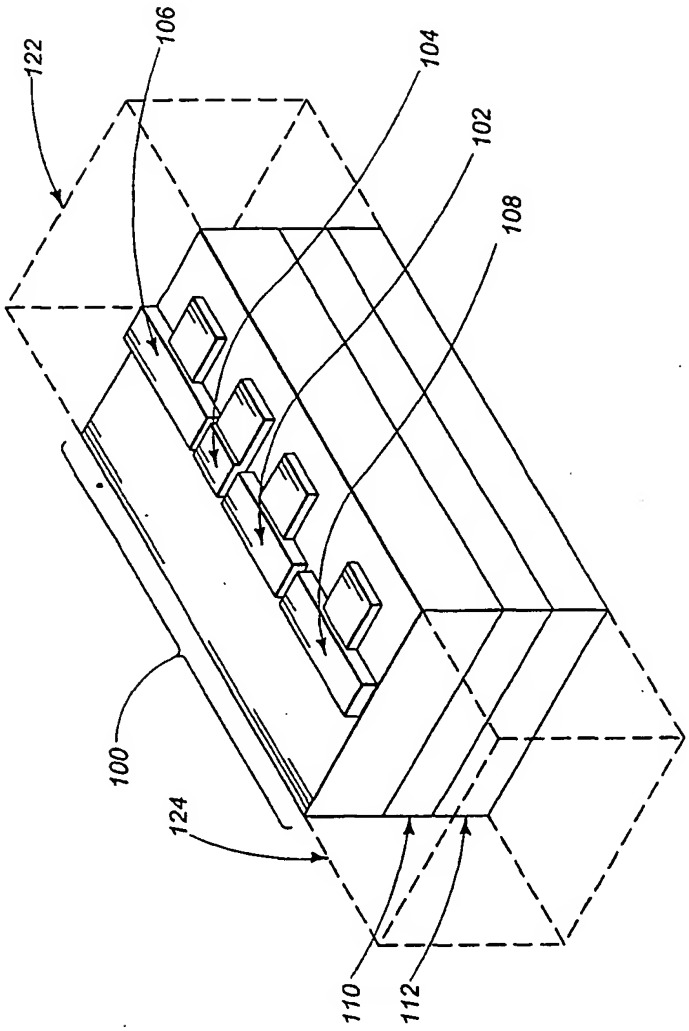


FIG. 1A

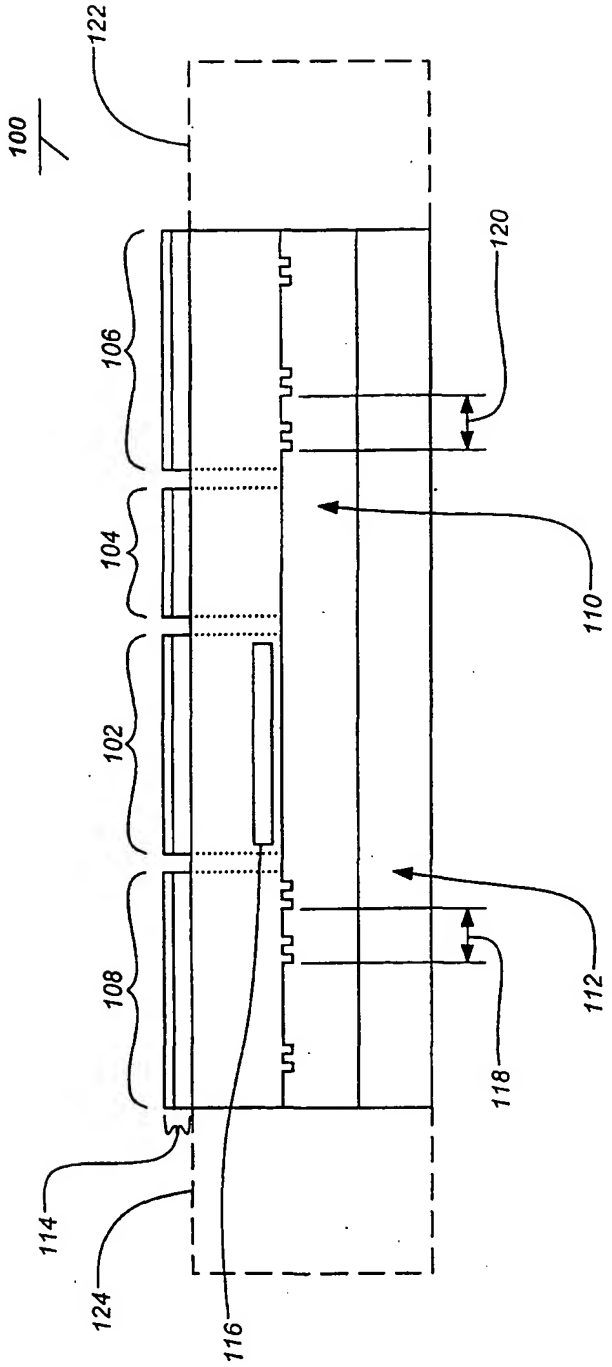


FIG. 1B

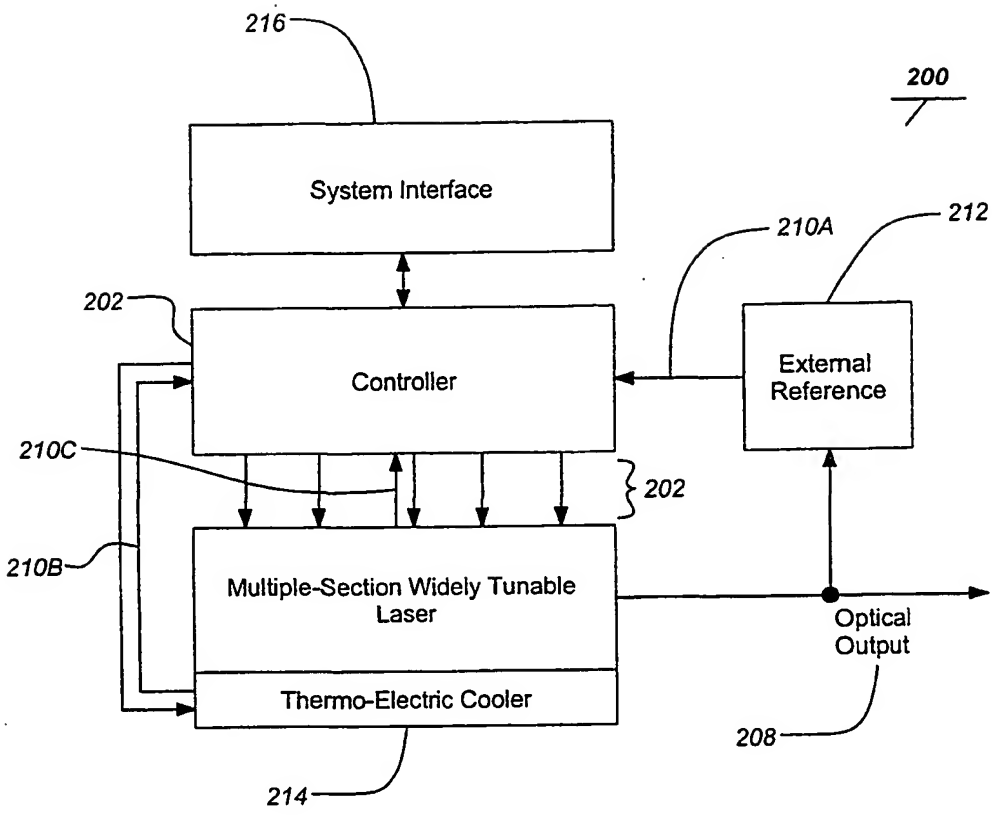
216
200
System Interface
210A
212
202
Controller
External Reference
210C
202
210B
Multiple-Section Widely Tunable Laser
Optical Output
Thermo-Electric Cooler
208
214

FIG. 2

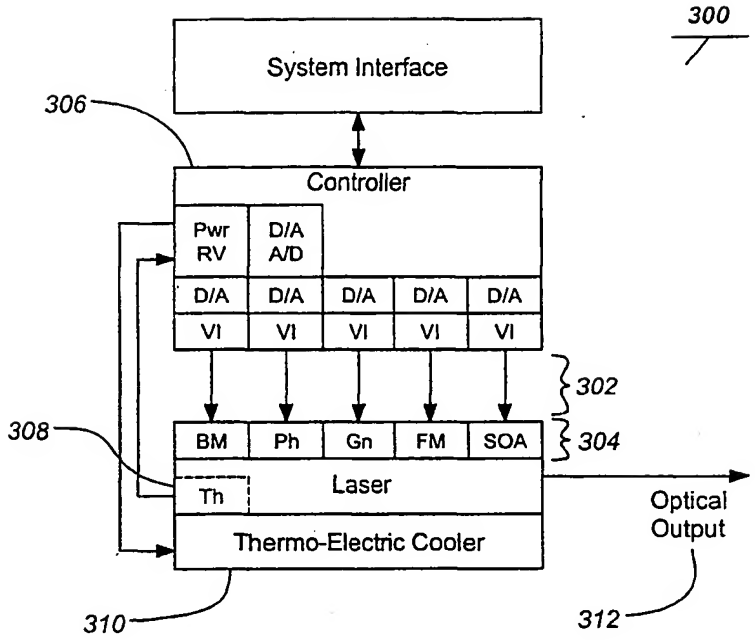
300
System Interface
306
Controller
Pwr RV
D/A A/D
D/A
VI
302
304
BM
Ph
Gn
FM
SOA
308
Th
Laser
Optical Output
Thermo-Electric Cooler
310
312

FIG. 3

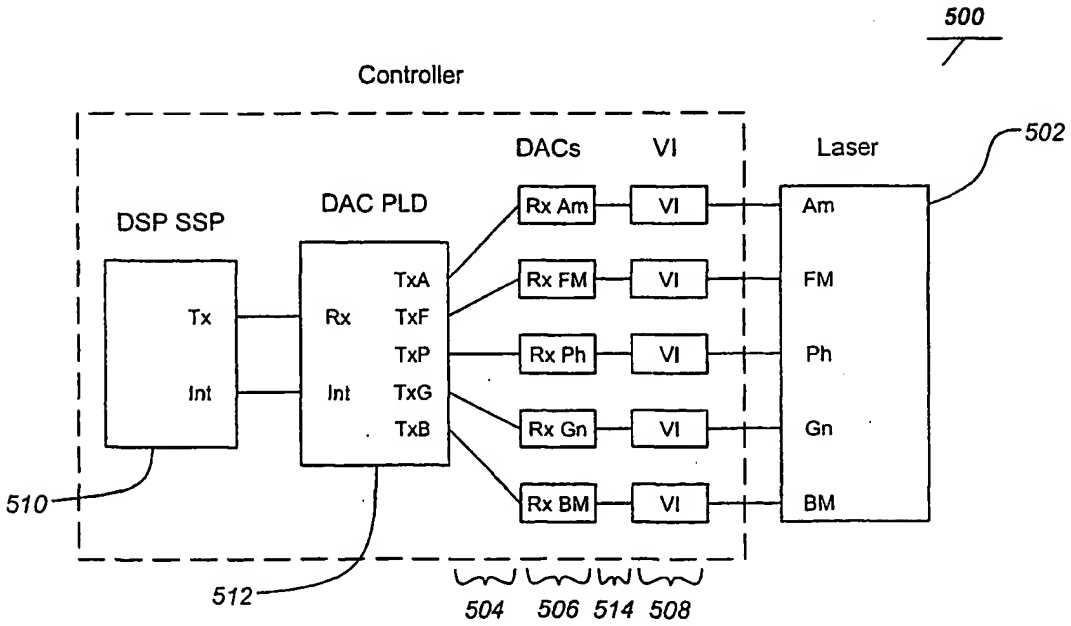
500
Controller
DACs
VI
Laser
502
DSP SSP
DAC PLD
Rx Am
Rx FM
Rx Ph
Rx Gn
Rx BM
Am
FM
Ph
Gn
BM
Tx
Int
Rx
TxA
TxF
TxP
TxG
TxB
510
512
504
506
514
508

FIG. 5

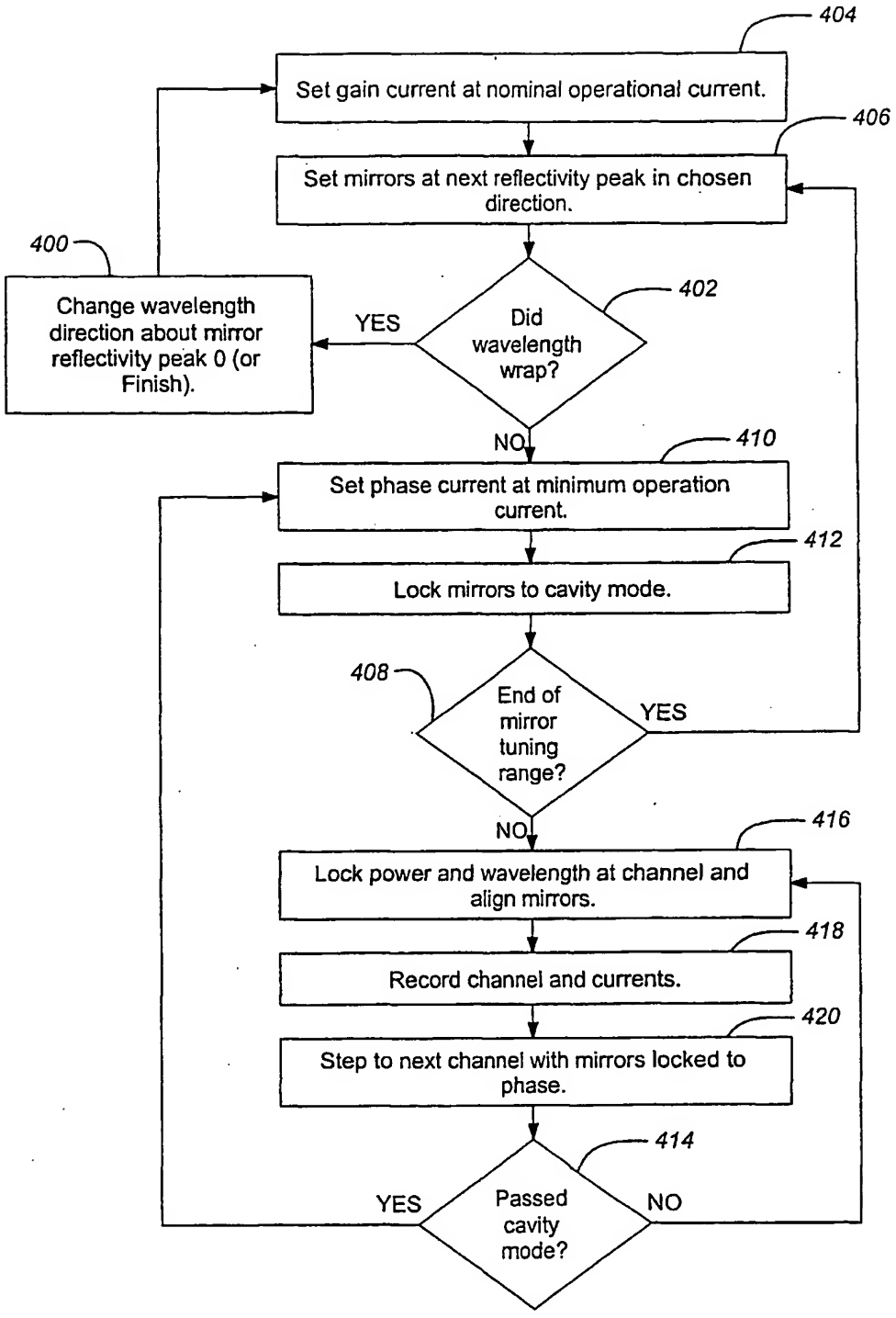
404
Set gain current at nominal operational current.
406
Set mirrors at next reflectivity peak in chosen direction.
400
Change wavelength direction about mirror reflectivity peak 0 (or Finish).
YES
402
Did wavelength wrap?
NO
410
Set phase current at minimum operation current.
412
Lock mirrors to cavity mode.
408
End of mirror tuning range?
YES
NO
416
Lock power and wavelength at channel and align mirrors.
418
Record channel and currents.
420
Step to next channel with mirrors locked to phase.
414
YES
Passed cavity mode?
NO

FIG. 4A

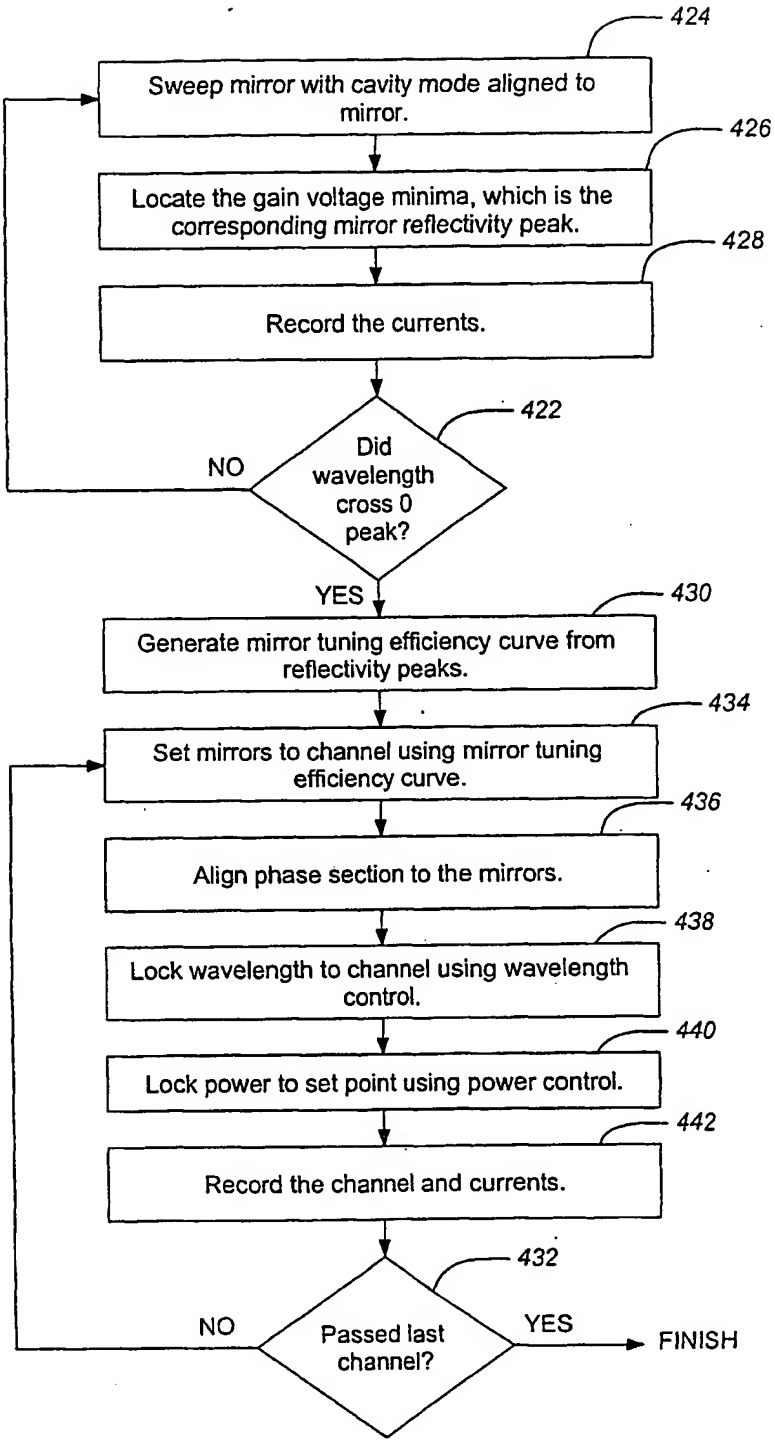
424
Sweep mirror with cavity mode aligned to mirror.
426
Locate the gain voltage minima, which is the corresponding mirror reflectivity peak.
428
Record the currents.
422
Did wavelength cross 0 peak?
NO
YES
430
Generate mirror tuning efficiency curve from reflectivity peaks.
434
Set mirrors to channel using mirror tuning efficiency curve.
436
Align phase section to the mirrors.
438
Lock wavelength to channel using wavelength control.
440
Lock power to set point using power control.
442
Record the channel and currents.
432
Passed last channel?
NO
YES
FINISH

FIG. 4B

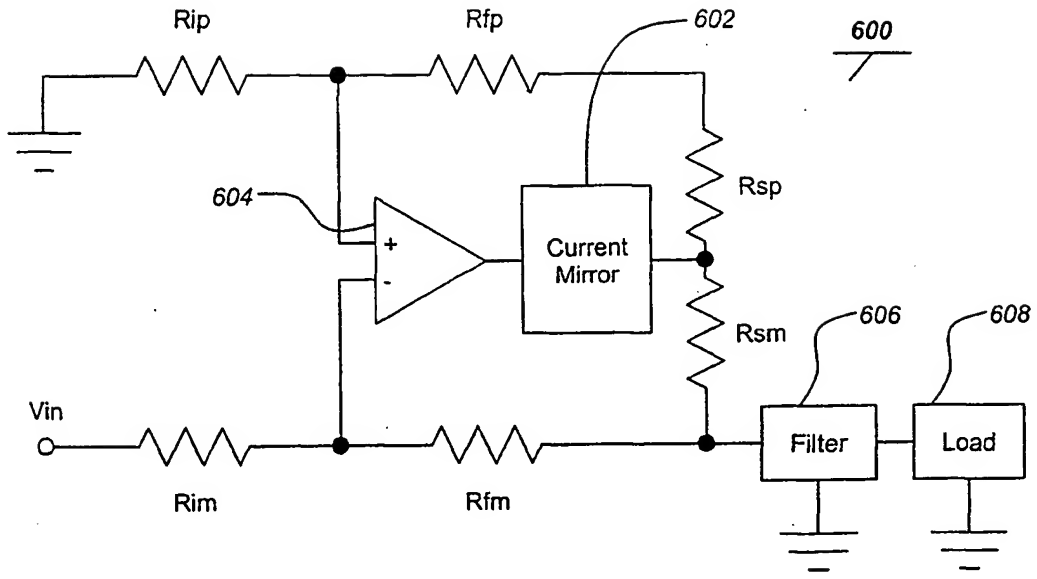
Rip
Rfp
602
600
604
Rsp
Current Mirror
Rsm
606
608
Vin
Filter
Load
Rim
Rfm

FIG. 6

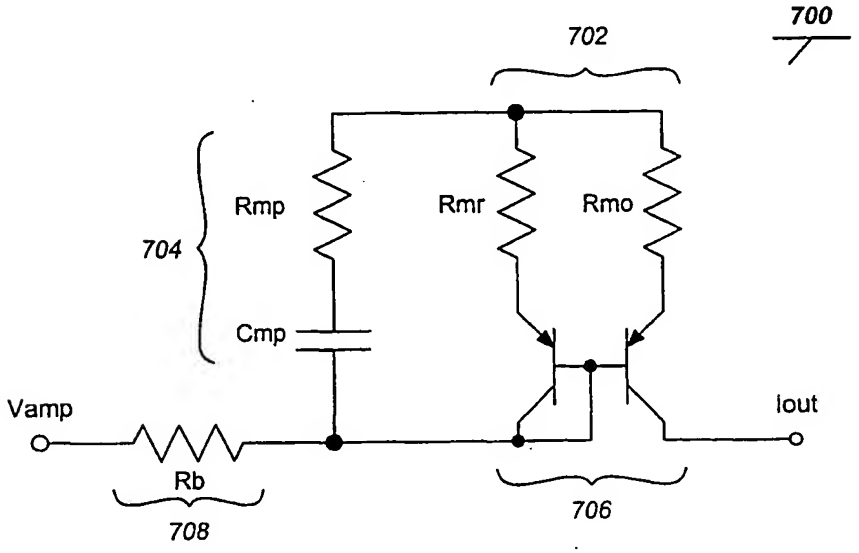
700
702
Rmp
Rmr
Rmo
704
Cmp
Vamp
Iout
Rb
708
706

FIG. 7

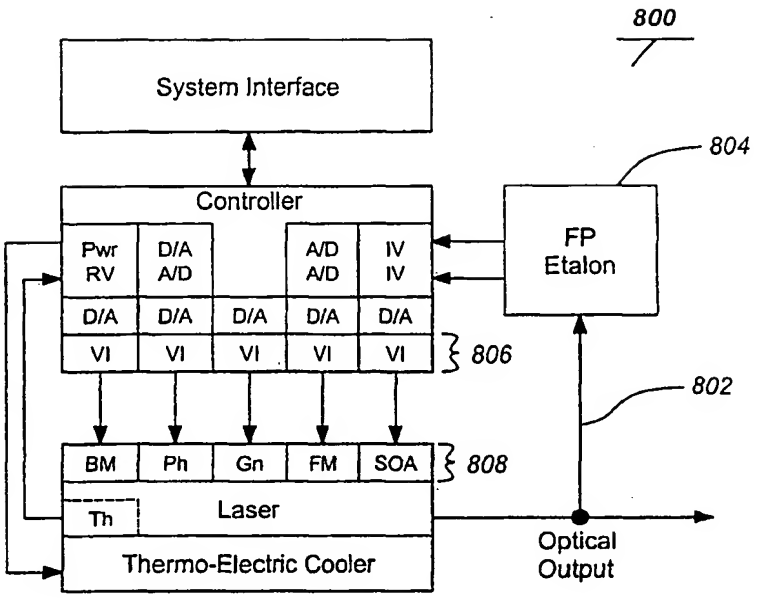
800
System Interface
804
Controller
Pwr RV
D/A A/D
A/D A/D
IV IV
FP Etalon
D/A
VI
806
802
BM
Ph
Gn
FM
SOA
808
Th
Laser
Thermo-Electric Cooler
Optical Output

FIG. 8A

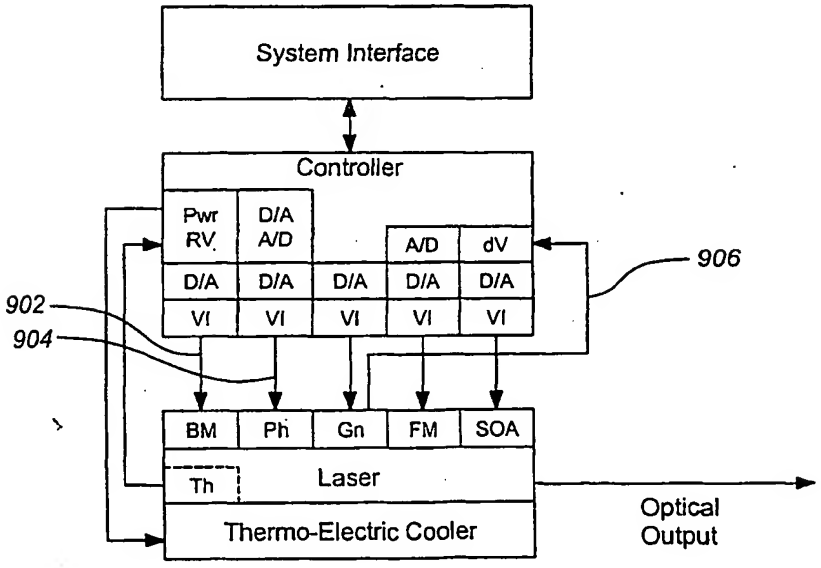
System Interface
Controller
Pwr RV
D/A A/D
A/D
dV
906
902
904
D/A
VI
BM
Ph
Gn
FM
SOA
Th
Laser
Thermo-Electric Cooler
Optical Output

FIG. 9

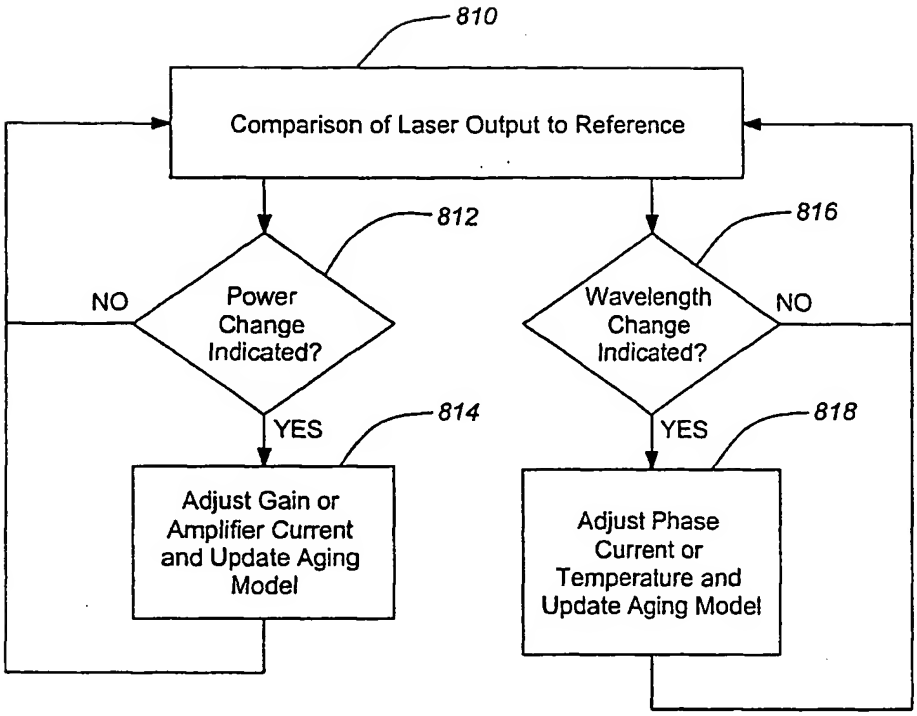
810
Comparison of Laser Output to Reference
812
Power Change Indicated?
NO
YES
814
Adjust Gain or Amplifier Current and Update Aging Model
816
Wavelength Change Indicated?
NO
YES
818
Adjust Phase Current or Temperature and Update Aging Model

FIG. 8B

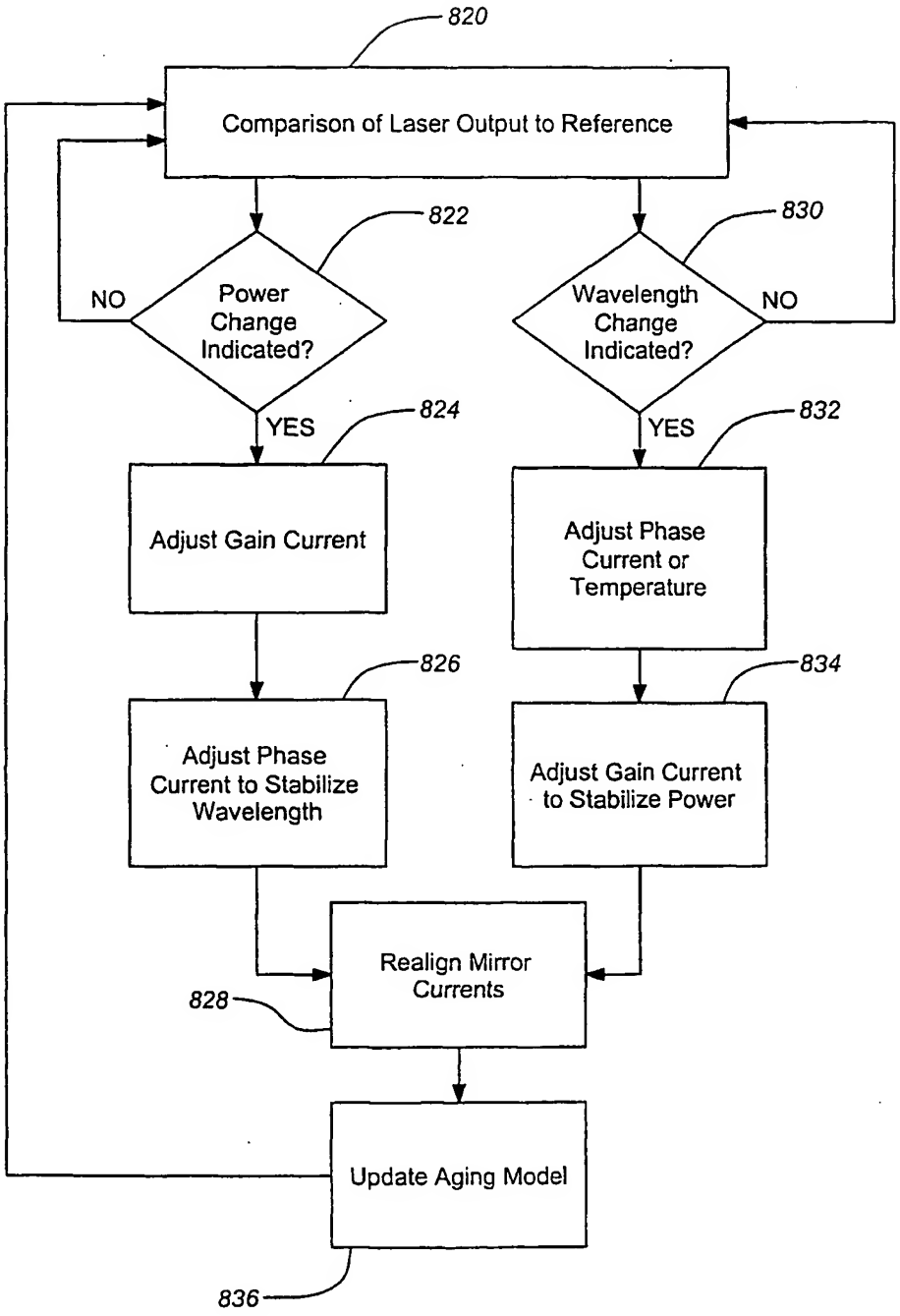
820
Comparison of Laser Output to Reference
822
Power Change Indicated?
NO
YES
824
Adjust Gain Current
826
Adjust Phase Current to Stabilize Wavelength
830
Wavelength Change Indicated?
NO
YES
832
Adjust Phase Current or Temperature
834
Adjust Gain Current to Stabilize Power
Realign Mirror Currents
828
Update Aging Model
836

FIG. 8C

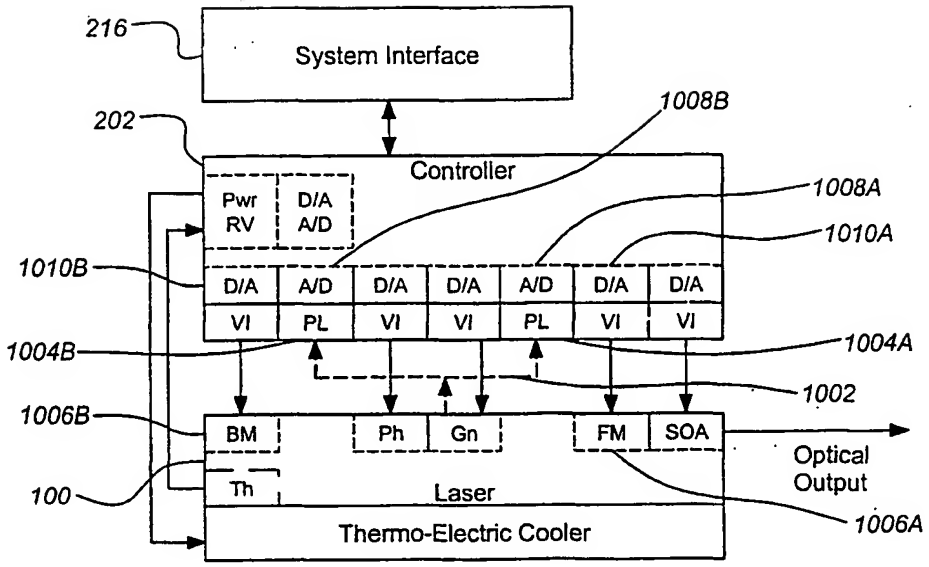
216
System Interface
202
1008B
Controller
Pwr
RV
D/A
A/D
1008A
1010A
1010B
D/A
A/D
D/A
D/A
A/D
D/A
D/A
VI
PL
VI
VI
PL
VI
VI
1004B
1004A
1002
1006B
BM
Ph
Gn
FM
SOA
Optical
Output
100
Th
Laser
1006A
Thermo-Electric Cooler

FIG. 10

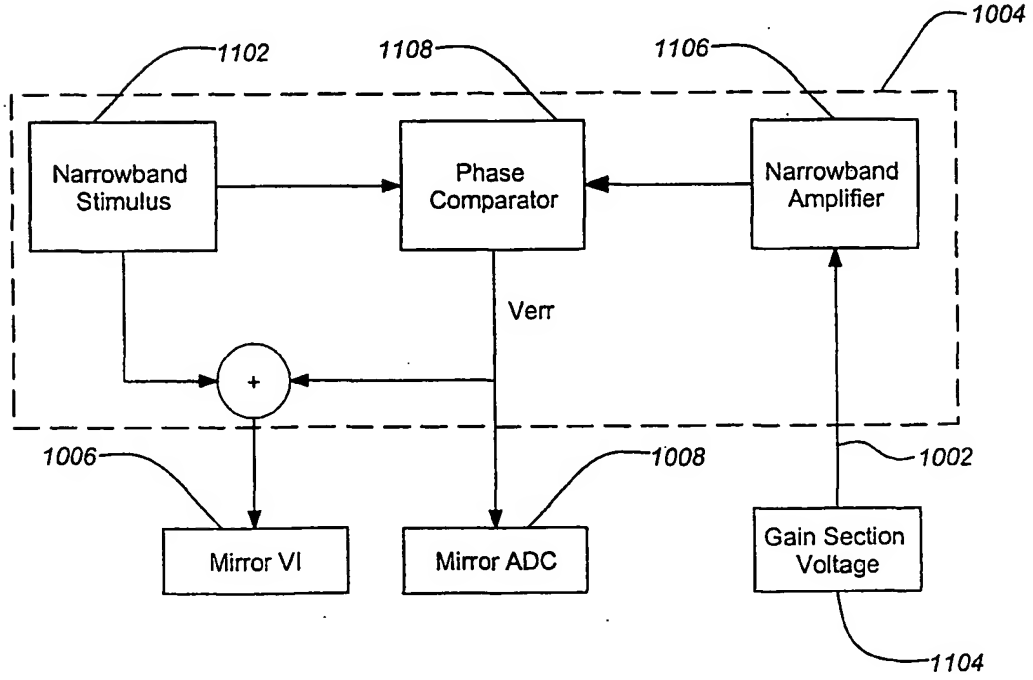
1004
1102
1108
1106
Narrowband
Stimulus
Phase
Comparator
Narrowband
Amplifier
Verr
+
1006
1008
1002
Mirror VI
Mirror ADC
Gain Section
Voltage
1104

FIG. 11

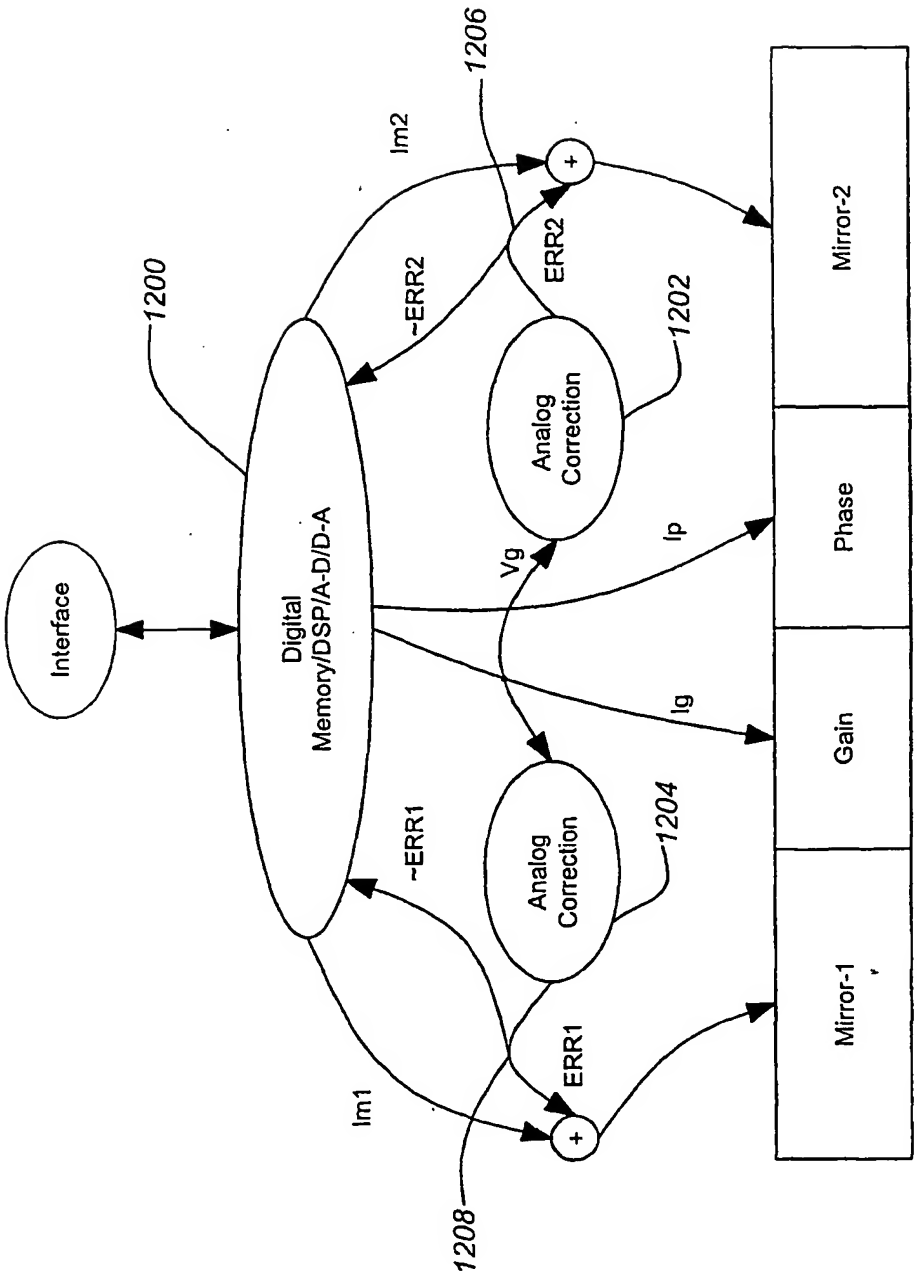
Interface
Digital Memory/DSP/A-D/D-A
1200
Im2
-ERR2
ERR2
1206
+
Analog Correction
1202
Vg
Ip
Ig
Mirror-2
Phase
Gain
Mirror-1
-ERR1
Analog Correction
1204
ERR1
Im1
+
1208

FIG. 12